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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,551	09/26/2003	Seiji Funaba	17072	3724

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EXAMINER	
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ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/672,551	FUNABA ET AL.	
	Examiner	Art Unit	
	BENJAMIN P. SANDVIK	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,7,11,13,14,17,19,23,25,31,35,68 and 74* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *13,14,17,19,23,25,31,35,68 and 74* is/are allowed.

6)☒ Claim(s) *1,2,5 and 7* is/are rejected.

7)☒ Claim(s) *11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin (U.S. Patent #6383916), in view of Shiraishi et al (U.S. PG Pub #2001/0002727), further in view of Towle et al (U.S. PG Pub #2002/0173133).

With respect to **claim 1**, Lin teaches a semiconductor unit having two device terminals for every one input/output signal (Fig. 10, 101-105 and 121-125), said semiconductor unit comprising: a laminated substrate (Fig. 10, 130 and Col 7 Ln 21-23, the substrate is multi-layer) comprising at least two wiring layers which include a signal wiring layer and a power-supply or ground wiring layer (Col 7 Ln 65-67), said laminated substrate having a main surface, a semiconductor chip (Fig. 10, 100) being mounted on the main surface of said laminated substrate, wherein said two device terminals are mounted on said laminated substrate and connected to both ends of a signal wire in said signal wiring layer (Fig. 10, 131), but does not explicitly disclose that said laminated substrate further comprises a via hole, with one end thereof connected to said signal wire and the other end thereof connected to said input/output pad of said

semiconductor chip. Shiraishi teaches a substrate wherein the wiring layers are connected to the chip through a via hole (Fig. 4, 109 and Paragraph 44), including connection between a wiring layer and an input/output pad of a semiconductor chip (Fig. 4, 102). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use via holes in the substrate of Lin as taught by Shiraishi in order to achieve the predictable result of reducing wiring length.

Furthermore, Lin does not teach an input/output pad contacting said main surface of said laminated substrate. Towle teaches a semiconductor chip having an input/output pad (Fig. 13, 12), wherein the input/output pad contacts a main surface (Fig. 13, 16) of a laminated substrate (Fig. 13, 42/48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the chip package of Lin so that an input/output pad contact the main surface of the laminated substrate as taught by Towle in order to improve the cost benefit and sorting capabilities of the manufacturing process (Paragraph 12).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Shiraishi, and Towle, in view of Yew et al (U.S. Patent #6137164).

With respect to **claim 2**, Lin does not teach that the semiconductor chip comprises a circuit comprising at least one of an input buffer and an output buffer, an input protection resistor, and an electrostatic protection element. Yew

teaches a chip having a layer of polymeric chip coating material (Col 6 Ln 39-41). It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide a layer of polymeric chip coating material to the chip of Lin as taught by Yew in order to give the chip electrostatic protection.

Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Shiraishi, and Towle, in view of Devnani (U.S. Patent #6630628).

With respect to **claim 5**, Lin does not teach that the signal wiring layer forms a micro-strip line with the ground wiring layer in said laminated substrate, said ground wiring layer being disposed between said signal wiring layer and said semiconductor chip. Devnani teaches that the signal layer forms a micro strip line and that the ground wiring layer (Fig. 2, 140) is disposed between the signal layer (Fig. 2, 150) and the semiconductor chip (Fig. 2, 105). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the signal and ground layers of Lin as taught Devnani in order to optimize the wiring arrangement of the substrate.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin, Shiraishi, and Towle, in view of Tanahashi (U.S. Patent #6184477).

With respect to **claim 7**, Lin does not teach said signal wiring layer being sandwiched between the power-supply layer and the ground layer in said laminated substrate, said signal wiring layer forming a strip line with the power-supply layer or the ground layer. Tanahashi teaches a signal layer (Fig. 6, S1)

between a power layer (Fig. 6, P) and a ground layer (Fig. 6, G), the signal layer forming a strip line (Fig. 5, S1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to arranged the wiring layers of Lin as taught by Tanahashi in order to optimize the electrical characteristics of the device.

Allowable Subject Matter

Claims 13, 14, 17, 19, 23, 25, 31, 35, 68, and 74 are allowed.

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BENJAMIN P. SANDVIK whose telephone number is (571)272-8446. The examiner can normally be reached on Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/B. P. S./
Examiner, Art Unit 2826

/Sue A. Purvis/
Supervisory Patent Examiner, Art Unit 2826